

What is Claimed:

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2 1. A digital filter, comprising:
3 at least two multiple stage shift registers;
4 a plurality of multiplier corresponding in number to the number of stages
5 in the at least two multiple stage shift registers, each multiplier receiving as a first input
6 an output from a stage of the at least two multiple stage shift registers, each multiplier
7 producing an output that is a product of inputs thereto:
8 a tap weight shifter coupled to a tap weight source to receive tap weights,
9 the tap weight shifter coupled to provide a second input to each multiplier, the tap weight
10 shifter capable of circularly shifting tap weights; and
11 an adder for summing the multiplier outputs to provide a sum output.
- 1 2. A digital filter as recited in claim 1, further comprising:
2 a multiplier stage buffer for receiving and storing digital samples, outputs
3 from the multiple stage buffer being coupled to provide inputs to the at least two multiple
4 stage shift registers.
- 1 3. A digital filter as recited in claim 2, wherein the multiple stage
2 buffer is a serial-input, parallel-output buffer.
- 1 4. A digital filter as recited in claim 1, wherein tap weights received
2 by the tap weight shifter one bit wide.
- 1 5. A digital filter as recited in claim 1, wherein tap weights received
2 by the tap weights received by the tap weight shifter are more than one bit wide and
3 having a bit width that is no greater than a bit width of stages of the shift registers.
- 1 6. A digital filter as recited in claim 1, wherein the digital filter is
2 implemented in software.
- 1 7. A digital filter as recited in claim 1, wherein the digital filter is
2 implemented in an integrated circuit.
- 1 8. A digital filter as recited in claim 7, wherein the digital filter is
2 implemented in an application specific integrated circuit.
- 1 9. A digital filter as recited in claim 7, wherein the digital filter is
2 implemented in a digital signal processor.

1 10. A digital filter as recited in claim 7, wherein the digital filter is
2 implemented in a microcontroller.

1 11. A digital filter as recited in claim 7, wherein the digital filter is
2 implemented a microprocessor.

1 12. A digital filter as recited in claim 1, further comprising a tap
2 weight source from which to receive tap weights.

1 13. A digital filter as recited in claim 12, wherein the tap weight
2 source is random access memory.

1 14. A digital filter as recited in claim 12, wherein the tap weight
2 source is read-only memory.

1 15. A digital filter as recited in claim 12, wherein the tap weight
2 source is a processor.

1 16. A receiver including a digital filter comprising:
2 at least two multiple stage shift registers;
3 a plurality of multiplier corresponding in number to the number of stages
4 in the at least two multiple stage shift registers, each multiplier receiving as a first input
5 an output from a stage of the at least two multiple stage shift registers, each multiplier
6 producing an output that is a product of inputs thereto:
7 a tap weight shifter coupled to a tap weight source to receive tap weights,
8 the tap weight shifter coupled to provide a second input to each multiplier, the tap weight
9 shifter capable of circularly shifting tap weights; and

10 an adder for summing the multiplier outputs to provide a sum output.

1 17. A receiver as recited in claim 16, further comprising:
2 a multiplier stage buffer for receiving and storing digital samples, outputs
3 from the multiple stage buffer being coupled to provide inputs to the at least two multiple
4 stage shift registers.

1 18. A receiver as recited in claim 17, wherein the multiple stage buffer
2 is a serial-input, parallel-output buffer.

1 19. A receiver as recited in claim 16, wherein tap weights received by
2 the tap weight shifter one bit wide.

1 20. A receiver as recited in claim 16, wherein tap weights received by
2 the tap weight shifter are more than one bit wide and having a bit width that is no greater
3 than a bit width of stages of the shift registers.

1 21. A receiver as recited in claim 16, wherein the digital filter is
2 implemented in software.

1 22. A receiver as recited in claim 16, wherein the digital filter is
2 implemented in an integrated circuit.

1 23. A receiver as recited in claim 22, wherein the digital filter is
2 implemented in an application specific integrated circuit.

1 24. A receiver as recited in claim 22, wherein the digital filter is
2 implemented in a digital signal processor.

1 25. A receiver as recited in claim 22, wherein the digital filter is
2 implemented in a microcontroller.

1 26. A receiver as recited in claim 22, wherein the digital filter is
2 implemented a microprocessor.

1 27. A receiver as recited in claim 16, further comprising a tap weight
2 source from which to receive tap weights.

1 28. A receiver as recited in claim 27, wherein the tap weight source is
2 random access memory.

1 29. A receiver as recited in claim 27, wherein the tap weight source is
2 read-only memory.

1 30. A receiver as recited in claim 27, wherein the tap weight source is
2 a processor.

1 31. A receiver as recited in claim 16, wherein the receiver is a handset.

1 32. A receiver as recited in claim 16, wherein the receiver is a base
2 station.

1 33. A method of filtering digital data, comprising the steps of:

2 a. shifting digital data into first and second multiple stage shift
3 registers;

4 b. multiplying an output from each stage of the first and second
5 multiple stage shift registers by an associated, respective tap weight to produce a plurality
6 of products;

7 c. combining the plurality of products to form a sum

8 d. circularly shifting the tap weights; and

9 e. repeating steps b and c.

1 34. A method of filtering digital data as recited in claim 33, further
2 comprising the step of
3 shifting digital data into registers of a buffer prior to shifting the digital
4 data into first and second multiple stage shift registers.

1 35. A method of filtering data, comprising the steps of:

2 a. shifting data into N multiple stage shift registers, each of the N
3 multiple stage shift registers having at least L stages, N and L being integers, N being at
4 least 2;

5 b. multiplying an output from each of the at least L stages of the N
6 multiple stage shift registers by a corresponding tap weight to produce a plurality of
7 products;

8 c. combining the plurality of products to form a sum;

9 d. circularly shifting the tap weights;

10 e. repeating steps b, c, and d N-2 times;

11 f. repeating steps b and c again.

1 36. A method of filtering data, further comprising the steps of
2 following step f, repeating steps a through f.

1 37. A method of filtering data as recited in claim 35, further
2 comprising the step of shifting N pieces of data into registers of a buffer for temporary
3 storage prior to shifting the N pieces of data into respective ones of the N multiple stage
4 shift registers.